Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1.(currently amended) A resonant tunneling diode (RTD) using low band offset dielectric material as double barrier layers and having a vertical layer configuration comprising:

a substrate having a substantially planar horizontal surface;

a horizontally disposed configuration of vertical layers formed on said substrate, said layers being perpendicular to said horizontal surface, said configuration further comprising:

a quantum well layer formed of a semiconductor material by photolithographic patterning and etching, said layer being vertical, having parallel planar vertical sides and being formed to a first thickness;

a tunneling barrier layer formed by a process of CVD, ALD or sputtering, on each side of said quantum well layer, each said barrier layer being formed, to a second thickness, of a dielectric material characterized by a low band offset relative to the conduction band edge of said semiconductor material; and

an adjacent conducting contact layer being formed on each said tunneling barrier layer.

2.(original) The RTD of claim 1 wherein said quantum well semiconductor material is monocrystalline Si, Ge or SiGe.

3.(original) The RTD of claim 1 wherein said quantum well layer is oriented so that its vertical sides are any preferred crystallographic plane.

4.(original) The RTD of claim 3 wherein said low band offset dielectric material is the high-k dielectric material Si_3N_4, HfO_2, ZrO_2, Y_2O_3, Pr_2O_3, TiO_2, Al_2O_3, or Ta_2O_5, or their alloys or laminates.

5.(original) The RTD of claim 4 wherein said dielectric material is formed to a second thickness of between approximately 0.5 nm. and 5.0 nm.

6.(original) The RTD of claim 5 wherein the quantum well layer is monocrystalline Si and the crystallographic planes are the 100, 110 or 111 crystallographic planes.

7.(original) The RTD of claim 6 wherein said Si quantum well layer is formed to a first thickness between approximately 2 nm. and 25 nm. and wherein said layer is characterized by at least one electron bound state and associated bound state energy.

8.(original) The RTD of claim 7 wherein the silicon quantum well layer is doped with either n-type or p-type doping to a dopant concentration between approximately 10^{16} and 10^{19} cm^{-3}.

9.(original) The RTD of claim 1 wherein each said conducting layer is a layer of n+ doped polysilicon or a layer of metal.

10.(original) The RTD of claim 1 wherein said substrate is a SOI, GOI or SiGe-on oxide substrate and wherein an isolating layer is interposed between said substrate and said horizontally disposed configuration.

Claims 11-51 are cancelled.